

### **Amendments to the Claims**

This listing of claims will replace all prior versions and listings of claims in the application:

#### **Listing of Claims:**

1. (currently amended) A method of fabricating a gate electrode for a semiconductor comprising the steps of:

providing a substrate prepared with a gate stack, the gate stack includes a gate dielectric on the substrate and a gate layer on the gate dielectric, the gate layer comprising a first material of thickness  $t_p$ , the first material being selected from the group consisting of Si,  $Si_{1-x}Ge_x$  alloy, Ge and mixtures thereof;

providing a metal layer on the gate layer, the metal layer having a thickness  $t_m$ , wherein the thicknesses  $t_p$  and  $t_m$  are related by a predetermined ratio of  $t_m/t_p$ ; and

annealing the layers, wherein the predetermined ratio results in such that all of the first material of the gate layer and substantially all of the metal of the metal layer over the gate layer are being consumed during reaction with one another to form a resulting layer which serves as the a gate electrode in contact with the gate dielectric, wherein the gate electrode comprises a work function close to about a mid-gap of silicon band gap.
2. (currently amended) The method of claim 1, wherein the metal layer comprises a metal selected from one of the group consisting of Ni, Pd, Pt, Co, [[Ti]] and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.

3. (previously presented) The method of claim 1, wherein the gate stack further comprises dielectric sidewall spacers and providing the metal layer comprises depositing the metal layer on the first material layer.

4. (cancelled)

5. (currently amended) The method of claim [[4]] 1, wherein the ratio of  $t_m/t_p$  is determined by the particular first material and metal to be annealed.

6. (original) The method of claim 1 wherein annealing is performed at temperatures ranging from 300 to 900°C.

7. (original) The method of claim 1 further comprising the step of depositing a further layer of metal on the gate electrode to increase gate thickness.

8. (original) The method of claim 7 comprising forming source/drain contacts simultaneously with the gate electrode.

9. (previously presented) The method of claim 7 , wherein as much as 5% of the metal remains following reaction with the other of the metal and the first material.

10. (currently amended) A gate electrode for a semiconductor device comprising:  
a substrate with a gate stack formed thereon, the gate stack includes a gate dielectric on  
the substrate and the gate electrode on the gate dielectric,  
wherein the gate electrode comprises a work function close to about a mid-gap of silicon  
band gap in which all of a first gate material and substantially all of a metal have been consumed  
during reaction with one another caused by annealing.

11. (currently amended) The gate electrode of claim 10, wherein the metal is  
selected from one of the group consisting of Ni, Pd, Pt, Co, [[Ti]] and alloys of these materials  
including Ni-Pt, Ni-Pd, Ni-Co.

12. (currently amended) The gate electrode of claim 10, wherein the first gate  
material is selected from the group consisting of Si,  $Si_{1-x}Ge_x$  alloy, Ge and mixtures thereof.

13. (previously presented) The gate electrode of claim 10 wherein as much as 5% of  
the metal remains following reaction with the other of the metal and the first material.

14. (previously presented) The gate electrode of claim 13, wherein a layer of metal is  
provided on the first material.

15. (original) The gate electrode of claim 10 wherein the gate electrode is incorporated  
in a CMOS semiconductor device.

16. (currently amended) A method for forming an integrated circuit comprising:  
providing a substrate prepared with a first gate stack with dielectric sidewall spacers on the substrate and first and second diffusion regions in the substrate adjacent to the gate stack, the gate stack includes a gate dielectric on the substrate and a gate layer on the gate dielectric,  
the gate layer comprises an amorphous or polycrystalline material having a thickness  $t_p$ ;  
depositing a metal layer over the substrate covering the gate stack and diffusion regions, the metal layer having a thickness  $t_m$ , wherein the thicknesses  $t_p$  and  $t_m$  are related by a predetermined ratio of  $t_m/t_p$ ; and  
processing the metal layer to cause a reaction between the gate layer and the metal layer, wherein the predetermined ratio results in such that all the material of the gate layer and portions of the metal layer over the gate layer are being consumed to form a resulting layer having a work function close to a mid gap of silicon band gap which serves as the gate electrode which contacts the gate dielectric,  
wherein problems associated with inversion and agglomeration associated with formation of the transistor are reduced.

17. (previously presented) The method of claim 16 wherein:  
the substrate is prepared with at least first and second gate stacks with dielectric sidewall spacers on the substrate and first and second diffusion regions in the substrate adjacent to the gate stacks, the gate stacks include a gate dielectric on the substrate and a gate layer on the gate dielectric, the first and second gate stacks serving as a first PMOS transistor and a first NMOS transistor to form a CMOS integrated circuit; and  
the material of the gate layer comprises silicon, germanium, alloys or a combination thereof, including  $\text{Si}_{1-x}\text{Ge}_x$ .

18. (previously presented) The method of claim 16 wherein the material of the gate layer comprises silicon, germanium, alloys or a combination thereof, including  $\text{Si}_{1-x}\text{Ge}_x$ .

19. (currently amended) The method of claim 17 wherein a metal material of the metal layer is selected from one of the group consisting of Ni, Pd, Pt, Co, [[Ti]] and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.

20. (previously presented) The method of claim 16 wherein processing the metal layer comprises annealing or rapid thermal annealing.

21. (previously presented) The method of claim 20 wherein unreacted metal layer is less than or equal to 10%.

22. (previously presented) The method of claim 16 wherein processing the metal layer also forms silicide over the diffusion regions.

23. (original) The method of claim 22 wherein processing the metal layer comprises annealing or rapid thermal annealing.

24. (previously presented) The method of claim 23 wherein unreacted metal layer is less than or equal to 10%.

25. (currently amended) The method of claim 16 wherein a metal material of the metal layer comprises Ni, Pd, Pt, Co, [[Ti,]] or a combination of alloys thereof including Ni-Pt, Ni-Pd, and Ni-Co.

26. (previously presented) The method of claim 25 wherein processing the metal layer also forms silicide over the diffusion regions.

27. (original) The method of claim 26 wherein processing the metal layer comprises annealing or rapid thermal annealing.

28. (original) The method of claim 25 wherein processing the metal layer comprises annealing or rapid thermal annealing.

29 – 32. (cancelled)

33. (previously presented) The method of claim 16 further comprises etching remaining portion of unreacted metal layer above the gate electrode after processing the metal layer.

34. (original) The method of claim 33 wherein processing the metal layer comprises annealing.

35. (previously presented) The method of claim 33 wherein processing the metal layer also forms silicide over the diffusion regions.

36. (original) The method of claim 35 wherein processing the metal layer comprises annealing or rapid thermal annealing.

37 - 40. (cancelled)

41. (previously presented) An integrated circuit comprising:  
a transistor disposed on a substrate, the transistor having  
a gate stack with a gate dielectric disposed on the substrate and a gate electrode  
disposed on and in contact with the gate dielectric, and  
first and second diffusion regions adjacent to the gate stack,  
the gate electrode is formed from an amorphous or polycrystalline first layer and a metal  
layer in which all of the first layer and substantially all of the metal layer have been consumed  
during reaction with one another caused by annealing, wherein problems associated with  
inversion and agglomeration associated with formation of the transistor are reduced.

42. (currently amended) A method of fabricating a gate electrode for a semiconductor  
comprising the steps of:

providing a substrate prepared with a gate stack, the gate stack includes a gate dielectric  
on the substrate and a gate layer on the gate dielectric, the gate layer comprising a first material  
of thickness  $t_p$ , the first material being selected from the group consisting of Si,  $Si_{1-x}Ge_x$  alloy,  
Ge and mixtures thereof;

providing a metal layer on the gate layer, the metal layer having a thickness  $t_m$ , wherein  
the thicknesses  $t_p$  and  $t_m$  are related by a predetermined ratio of  $t_m/t_p$ ; and

annealing the layers, such that wherein the predetermined ratio results in substantially all of the first material of the gate layer and metal of the metal layer over the gate layer are being consumed during reaction with one another to form a resulting layer which serves as the gate electrode in contact with the gate dielectric, wherein source/drain contacts are formed simultaneously with the gate electrode.